

MEMORY DEVICE AND METHOD HAVING DATA PATH WITH MULTIPLE
PREFETCH I/O CONFIGURATIONS

ABSTRACT OF THE DISCLOSURE

A memory device is operable in either a high mode or a low speed mode. In either mode, 32 bits of data from each of two memory arrays are prefetched into respective sets of 32 flip-flops. In the high-speed mode, the prefetched data bits are transferred in parallel to 4 parallel-to-serial converters, which transform the parallel data bits to a burst of 8 serial data bits and apply the burst to a respective one of 4 data bus terminals. In the low speed mode, two sets of prefetched data bits are transferred in parallel to 8 parallel-to-serial converters, which transform the parallel data bits to a burst of 8 serial data bits and apply the burst to a respective one of 8 data bus terminals.